Scott Beamer

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Interests

Computer architecture, systems, graph algorithms, memory interconnects

I design architectures, systems, and algorithms to improve *communication efficiency*, which in turn increases performance, decreases energy consumption, and ultimately reduces the cost for data-intensive applications. My approach utilizes both software optimization and hardware specialization.

Education

Ph.D. Computer Science, University of California, Berkeley, 2016
Thesis: Understanding and Improving Graph Algorithm Performance
Advisors: Krste Asanović and David Patterson
Outside Minor: Teaching

M.S. Computer Science, University of California, Berkeley, 2009
Thesis: Designing Multisocket Systems with Silicon Photonics

B.S. Electrical Engineering & Computer Science with Honors, University of California, Berkeley, 2007

Research Positions

Postdoctoral Fellow, Lawrence Berkeley National Laboratory, 2016 - present

Graduate Student Researcher, University of California, Berkeley, 2007 - 2016

Research Assistant, Massachusetts Institute of Technology, Summer 2006

Awards

Best Paper Award, International Parallel & Distributed Processing Symposium (IPDPS), May 2017

Kaivalya Dixit Distinguished Dissertation Award, Standard Performance Evaluation Corporation (SPEC), November 2016

Best Paper Award, International Symposium on Workload Characterization (IISWC), October 2015

Invited Paper, Journal of Scientific Programming, 2013

Best Student Paper Finalist, International Conference on High Performance Computing, Networking, Storage and Analysis (SC), November 2012

Outstanding Graduate Student Instructor, University of California, Berkeley, May 2011

Best Paper Finalist, International Symposium on Networks-on-Chip (NoCS), May 2009

Honorable Mention, NSF Graduate Research Fellowship Program, March 2008

Cisco Internet Generation Scholar, University of California, Berkeley, 2003 - 2007

Publications

Peer-Reviewed

Scott Beamer, Krste Asanović, David Patterson, "Reducing Pagerank Communication via Propagation Blocking," *International Parallel & Distributed Processing Symposium (IPDPS)*, Orlando, FL, May 2017. **Best Paper Award**.

Scott Beamer, Krste Asanović, David Patterson, "GAIL: The Graph Algorithm Iron Law," *Workshop on Irregular Applications: Architectures and Algorithms (IA^3), at the International Conference for High Performance Computing, Networking, Storage and Analysis (SC)*, Austin, TX, November 2015.

Scott Beamer, Krste Asanović, David Patterson, "Locality Exists in Graph Processing: Workload Characterization on an Ivy Bridge Server," *International Symposium on Workload Characterization (IISWC)*, Atlanta, GA, October 2015. **Best Paper Award**.

Scott Beamer, Krste Asanović, David Patterson, "Direction-Optimizing Breadth-First Search," *Journal of Scientific Programming*, 21(3-4), (invited paper), October 2013.

Scott Beamer, Aydın Buluç, Krste Asanović, David Patterson, "Distributed Memory Breadth-First Search Revisited: Enabling Bottom-Up Search," *Workshop on Multithreaded Architectures and Applications (MTAAP), at the International Parallel & Distributed Processing Symposium (IPDPS)*, Boston, MA, May 2013.

Scott Beamer, Krste Asanović, David Patterson, "Direction-Optimizing Breadth-First Search," *International Conference on High Performance Computing, Networking, Storage and Analysis (SC)*, Salt Lake City, Utah, November 2012. **Best Student Paper Finalist**.

Shoaib Kamil, Derrick Coetzee, Scott Beamer, Henry Cook, Ekaterina Gonina, Jonathan Harper, Jeffrey Morlan, and Armando Fox, "Portable Parallel Performance from Sequential, Productive, Embedded Domain-Specific Languages," *Symposium on Principles and Practice of Parallel Programming (PPoPP)*, New Orleans, Louisiana, February 2012.

Scott Beamer, Chen Sun, Yong-jin Kwon, Ajay Joshi, Christopher Batten, Vladimir Stojanović, Krste Asanović, "Re-Architecting DRAM Memory Systems with Monolithically Integrated Silicon Photonics," *International Symposium on Computer Architecture (ISCA)*, Saint-Malo, France, June 2010.

Vladimir Stojanović, Ajay Joshi, Christopher Batten, Yong-Jin Kwon, Scott Beamer, Sun Chen, and Krste Asanović, "A Design-Space Exploration for CMOS Photonic Processor Networks," *Optical Fiber Communication Conference and Exposition and The National Fiber Optic Engineers Conference (OFC/NFOEC)*, (invited paper), San Diego, CA, March 2010.

Ajay Joshi, Christopher Batten, Yong-Jin Kwon, Scott Beamer, Imran Shamim, Krste Asanović, and Vladimir Stojanović, "Limits and Opportunities for Designing Manycore Processor-to-Memory Networks using Monolithic Silicon Photonics," *Workshop on Photonic Interconnects & Computer Architecture (PICA), at the International Symposium on Microarchitecture (MICRO)*, New York, NY, December 2009.

Scott Beamer, Krste Asanović, Christopher Batten, Ajay Joshi, and Vladimir Stojanović, "Designing Multi-socket Systems Using Silicon Photonics," *International Conference on Supercomputing (ICS)*, Yorktown Heights, NY, June 2009.

Ajay Joshi, Christopher Batten, Yong-Jin Kwon, Scott Beamer, Imran Shamim, Krste Asanović; and Vladimir Stojanović, "Silicon-Photonic Clos Networks for Global On-Chip Communication," *International Symposium on Networks-on-Chip (NoCS)*, San Diego, CA, May 2009. **Best Paper Finalist**.

Theses

Scott Beamer, "Understanding and Improving Graph Algorithm Performance," *Ph.D. Thesis*, University of California Berkeley, Tech Report 2016-153, September 2016. **SPEC Kaivalya Dixit Distinguished Dissertation Award**

Scott Beamer, "Designing Multisocket Systems with Silicon Photonics," *M.S. Thesis*, University of California Berkeley, Tech Report 2009-189, December 2009.

Technical Reports

Krste Asanović, Rimas Avižienis, Jonathan Bachrach, Scott Beamer, et al., "The Rocket Chip Generator," *Technical Report UCB/EECS-2016-17, University of California, Berkeley*, April 2016.

Scott Beamer, Krste Asanović, David Patterson, "The GAP Benchmark Suite," *arXiv:1508.03619*, August 2015.

Scott Beamer, Krste Asanović, David Patterson, "Searching for a Parent Instead of Fighting Over Children: A Fast Breadth-First Search Implementation for Graph500," *Technical Report UCB/EECS-2011-117, University of California, Berkeley*, November 2011.

Book Chapters

Aydın Buluç, Scott Beamer, Kamesh Madduri, Krste Asanović, and David Patterson. "Distributed-Memory Breadth-First Search on Massive Graphs." In David Bader, editor, *Parallel Graph Algorithms*. CRC Press, Taylor-Francis, 2018 (in press).

Invited Presentations

Underappreciated Bottlenecks for Graph Algorithm Communication

SIAM Parallel Processing, Tokyo, Japan, (to appear) March 2018

Communication Challenges & Opportunities for Graph Processing

Georgia Tech, Atlanta, September 2017

Understanding and Improving Graph Algorithm Performance

International Conference on Performance Engineering (ICPE), L'Aquila, Italy, April 2017

Graph Processing Bottlenecks

Cavium Inc., San Jose, January 2016

University of Texas, Austin, November 2015

Workshop for Computer Architecture for Machine Learning (CAMEL), at the International Symposium on Computer Architecture (ISCA), June 2015

Searching for a Parent Instead of Fighting Over Children: A Fast Breadth-First Search Implementation for Graph 500

Sandia National Labs, April 2012

NVIDIA, March 2012

Designing Multisocket Systems Using Silicon Photonics

MIT CIPS Annual Meeting, May 2009

Teaching Experience

Great Ideas in Computer Architecture (Machine Structures), CS 61c, University of California, Berkeley

Course Instructor, Summer 2007
Head Teaching Assistant, Fall 2006, Spring 2010
Teaching Assistant, Spring 2012
Lab Assistant, Spring 2005, Fall 2005, Spring 2006
Curriculum Redesign Committee, Spring 2010

Computer Architecture and Engineering, CS 152, University of California, Berkeley

Teaching Assistant, Spring 2009

Graduate Student Instructor Conference, University of California, Berkeley

Computer Science Workshop Instructor, Fall 2013, Fall 2014, Fall 2015

Training Completed, University of California, Berkeley

CS 301: Teaching Techniques for Computer Science, Fall 2006
CS 302: Designing Computer Science Education, Spring 2010
SCMATHE 220C: Designing Educational Technologies, Spring 2012

Service

Program Committee

Early Career Program, International Conference on High Performance Computing, Networking, Storage and Analysis (SC) 2017
High Performance Graph Data Management and Processing Workshop (HPGDMP), 2016
International Parallel & Distributed Processing Symposium (IPDPS), 2018
Workshop on Irregular Applications: Architectures and Algorithms (IA^3), 2015, 2016, 2017
Workshop on Architecture for Graph Processing (AGP), 2017

External Program Committee

International Symposium for Computer Architecture (ISCA), 2017

External Reviewer

Computer Architecture Letters (CAL), 2015
Computing (COMP), 2017
IEEE Computer, 2015
IEEE Design & Test (DT), 2017
Information Processing Letters (IPL), 2013
International European Conference on Parallel and Distributed Computing (Euro-Par), 2014
International Symposium for Computer Architecture (ISCA), 2013
Journal of Experimental Algorithmics (JEA), 2014

Journal of Parallel and Distributed Computing (JPDC), 2014

Symposium on Parallelism in Algorithms and Architectures (SPAA), 2015

Transactions on Knowledge and Data Engineering (TKDE), 2016

Transactions on Multi-Scale Computing Systems (MSCS), 2017

Transactions on Parallel and Distributed Systems (TPDS), 2014, 2015

Graduate Admissions Reviewer, Computer Science Division, University of California, Berkeley, 2014

EECS Peer Advisor, University of California, Berkeley, 2013 - 2016

Industry Experience

Nokia Research, *Research Intern*, Berkeley, CA, Summer 2010
Modeled and measured power of mobile devices. Investigated feasibility of adoption and best uses for phase-change memory in mobile devices.

Google Inc., *Network Security Intern*, Mountain View, CA, Summer 2008
Researched and implemented a system to detect botnets by correlating network traffic based solely on network flow information.

Cisco Systems Inc., *Test Engineering Intern*, San Jose, CA, Summer 2005
Designed and implemented utilities and test cases for an automated testing framework targeting a web-based application. Driving consumer was an IP Telephony management service.

Cisco Systems Inc., *Network Management Intern*, San Jose, CA, Summer 2004
Helped support a Network Management lab with a wide variety of network hardware. In spare time, studied for and passed exam for a Cisco Certified Network Associate.

Open-Source Contributions

GAP Benchmark Suite - Created and maintained a high-performance reference implementation for the GAP Benchmark. For many of the kernels (BFS & SSSP), the implementations are the fastest available. The codebase has been used by others to characterize graph workloads, evaluate graph hardware accelerators, and compare performance of software graph frameworks.

BFS Releases - Contributed implementations of my direction-optimizing breadth first search algorithm to two existing codebases: the reference code for Graph 500 and the CombBLAS framework.

RISC-V Ecosystem - RISC-V is an free and open ISA originally developed at UC Berkeley that has transformed into a standard supported by a foundation with fifty member companies and numerous silicon implementations both from research and industry. Rocket Chip is an open-source RISC-V SoC generator also originally developed at UC Berkeley, and it has since been adopted both by research and industry. I contributed to both projects. In addition to debugging and supporting the RISC-V toolchain, I ported it to macOS. I also created the infrastructure to host Rocket Chip on an FPGA, and this harness was the foundation for multiple projects.

References

Krste Asanović
Professor, Computer Science Division
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David Patterson
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University of California, Berkeley
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Vladimir Stojanović
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